CLAIMS

What is claimed is:

1. A memory circuit, comprising:

a magnetoresistive random access memory (MRAM) core for storing data received by the memory circuit and outputting stored data, the magnetoresistive random access memory (MRAM) having a reserved portion;

an error correction code (ECC) coder for adding a redundancy code to the data for storing in the magnetoresistive random access memory (MRAM) core;

an ECC corrector, coupled to the magnetoresistive random access memory (MRAM) core, for performing an analysis of the stored data and the redundancy code to detect and correct errors in the stored data that is output by the magnetoresistive random access memory (MRAM) core and providing an error signal when an error is detected from the analysis; and

an error counter, coupled to the ECC corrector and the magnetoresistive random access memory (MRAM) core, for providing a count of occurrences of the error signal for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core.

2. The memory circuit of claim 1, wherein the error counter is coupled to the magnetoresistive random access memory (MRAM) core by the ECC coder.

3. The memory circuit of claim 1, further comprising a write cycle counter for providing a count of occurrences of writing data in the

magnetoresistive random access memory (MRAM) core for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core.

4. The memory circuit of claim 3, further comprising a read cycle counter for providing a count of occurrences of reading data from the magnetoresistive random access memory (MRAM) core for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core.

5. The memory circuit of claim 4, wherein the read cycle counter and the write cycle counter are coupled to the magnetoresistive random access memory (MRAM) core by the ECC coder.

6. The memory circuit of claim 1, further comprising control means for initiating writing the count of the error counter during an end portion of a read cycle and completing writing the count of the error counter before or during a beginning portion of a cycle immediately following the read cycle.

7. The memory circuit of claim 6, wherein the control means causes performance of a read operation, a compare operation, and a toggle operation to perform a write cycle.

8. A memory circuit, comprising:

a non-volatile random access memory (NVRAM) core for storing data received by the memory circuit and outputting stored data;

an ECC corrector, coupled to the non-volatile random access memory (NVRAM) core, for performing an analysis of stored data fetched from the non-volatile random access memory (NVRAM) core during a read cycle of the non-volatile random access memory (NVRAM) core to detect and correct errors in the stored data that is output by the non-volatile random access memory (NVRAM) core and providing an error signal when an error is detected from the analysis; and

an error counter, coupled to the ECC corrector and the non-volatile random access memory (NVRAM) core, for providing a count of occurrences of the error signal for storage in the non-volatile random access memory (NVRAM) core.

9. The memory circuit of claim 8, further comprising an ECC coder, coupled to the non-volatile random access memory (NVRAM) core, for adding a redundancy code to the data for storing in the non-volatile random access memory (NVRAM) core.

10. The memory circuit of claim 9, wherein the ECC corrector is further characterized as performing an analysis of the redundancy code to detect and correct errors.

11. The memory circuit of claim 10, wherein the non-volatile random access memory (NVRAM) core has a reserved portion and the count of the error counter is stored in the reserved portion.

12. The memory circuit of claim 9, wherein the error counter is coupled to the non-volatile random access memory (NVRAM) core by the ECC coder.

13. The memory circuit of claim 9, further comprising a write cycle counter for providing a count of occurrences of writing data in the non-volatile random access memory (NVRAM) core for storage in the non-volatile random access memory (NVRAM) core.

14. The memory circuit of claim 13, further comprising a read cycle counter for providing a count of occurrences of reading data from the non-volatile random access memory (NVRAM) core for storage in the non-volatile random access memory (NVRAM) core.

15. The memory circuit of claim 14, wherein the read cycle counter and the write cycle counter are coupled to the non-volatile random access memory (NVRAM) core by the ECC coder.

16. The memory circuit of claim 8, wherein the non-volatile random access memory (NVRAM) core is a magnetoresistive random access memory core, and further comprises control means for initiating writing the count of the error counter during an end portion of a read cycle and completing writing the count of the error counter before or during a beginning portion of a cycle immediately following the read cycle.

17. The memory circuit of claim 16, wherein the control means causes performance of a read operation, a compare operation, and a toggle operation to perform a write cycle.

18. A method of operating a memory circuit having a non-volatile random access memory (NVRAM) core, comprising:

storing data received by the memory circuit in the non-volatile random access memory (NVRAM) core;

outputting the data stored in the non-volatile random access memory (NVRAM) core;

performing an analysis of the data output from the non-volatile random access memory (NVRAM) core to detect and correct errors therein;

obtaining a count of detected errors; and

storing the count in the non-volatile random access memory (NVRAM) core.

19. The method of claim 18, further comprising:

storing a redundancy code with the data in the non-volatile random access memory (NVRAM) core.

20. The method of claim 19, wherein the performing the analysis further comprises analyzing the redundancy code.

21. The method of claim 20, wherein storing the count further comprises:

initiating the storing of the count during an end portion of a next read cycle of the memory circuit after an error has been detected; and

completing the storing of the count before or during an initial portion of a cycle immediately following the next read cycle.

22. The method of claim 21 further comprising implementing the non-volatile random access memory (NVRAM) core as a magnetoresistive random access memory core and implementing the cycle immediately

following the next read cycle as a write cycle, wherein the write cycle comprises a read operation, a compare operation, and a toggle operation.

23. The method of claim 18 further comprising implementing the non-volatile random access memory (NVRAM) core with bit cells having storage values that are changed by toggling their state.

24. The method of claim 18, further comprising:

obtaining a count of read cycles;

storing the count of read cycles in the non-volatile random access memory (NVRAM) core;

obtaining a count of write cycles; and

storing the count of write cycles in the non-volatile random access memory (NVRAM) core.

25. The method of claim 24, further comprising:

comparing the count of detected errors to the count of write cycles.

26. The method of claim 24, further comprising:

comparing the count of detected errors to the count of read cycles.

27. The method of claim 24, further comprising:

comparing the count of detected errors to a sum of the count of read cycles and the count of write cycles.